IN THE CLAIMS

Claims 1-33 (Cancelled)

34. (Currently amended) A processing device, comprising:

a reconfigurable circuit allowing change in function and connection relation;

a setting portion storing setting data representing a divided unit forming a part of an intended circuit, and supplying the setting data to said reconfigurable circuit; and

a control portion controlling said setting portion such that a plurality of setting data are successively supplied ~~according to a process flow~~ to said reconfigurable circuit to configure said intended circuit; wherein

said reconfigurable circuit has N ~~at least one~~ state holding circuits ~~circuit~~ holding an internal state;

said reconfigurable circuit is divided, by an arrangement of said N state holding circuits ~~circuit~~, into (N+1) ~~a plurality of~~ stages of reconfigurable units; ~~and~~

said control portion controls said setting portion such that, when a plurality of intended circuits are to be configured, setting data for configuring divided units each forming a part of the circuits on respective ones of said plurality of stages of reconfigurable units are successively supplied along a process flow,

said control portion controls ~~at one time point,~~ said setting portion such that at one time point, setting data of a divided unit configuring an intended circuit is supplied to the [[a]] reconfigurable unit between i-th state holding circuit and (i+1)th state holding circuit ~~at a predetermined stage~~,

~~at a next time point,~~

said control portion controls said setting portion such that at a next time point, setting data of a next divided unit configuring said intended circuit is supplied to the ~~said~~ reconfigurable unit between the (i+1)th state holding circuit and (i+2)th state holding circuit in accordance with the process flow, and ~~at a stage next to said predetermined stage,~~

said control portion controls said setting portion such that at said next time point, setting data of a divided unit configuring a ~~circuit~~ different ~~from said~~ intended circuit is supplied to the ~~said~~ reconfigurable unit between the i-th state holding circuit and the (i+1) state holding circuit. ~~of said predetermined stage;~~

~~said reconfigurable circuit including a path portion to input an output of the reconfigurable unit of the last stage to the reconfigurable unit of the first stage.~~

Claims 35-36 (Cancelled)

37. (Previously presented) The processing device according to claim 34, wherein a reconfigurable unit is configured as a combinational circuit.

38. (Previously presented) The processing device according to claim 34, further comprising:

an output circuit receiving an output of said reconfigurable circuit,

said output circuit providing the output of said reconfigurable circuit when said reconfigurable circuit is configured a plurality of times by said setting portion.

39. (Previously presented) The processing circuit according to claim 34, further comprising:

an internal state holding circuit receiving an output of said reconfigurable circuit; and

a first path portion inputting the output signal held by said internal state holding circuit to the first stage of reconfigurable units.

40. (Previously presented) The processing device according to claim 39, further comprising:

a memory portion storing in a prescribed area an output of said reconfigurable circuit in accordance with a setting data; and

a second path portion transmitting the output of the circuit configured on said reconfigurable circuit stored in said prescribed area of said memory portion as an input to a circuit configured in accordance with the next setting data.

41. (Previously presented) The processing circuit according to claim 40, further comprising:

a switching circuit switching between the input from said second path portion and an external input, to be an input to said reconfigurable circuit.

42. (Previously presented) The processing device according to claim 34, wherein

a reconfigurable unit includes a plurality of logic circuits each capable of selectively executing a plurality of operation functions, and a connecting portion allowing setting of connection relation among the logic circuits; and

said setting portion sets the functions and said connection relation of said logic circuits.

43. (Previously presented) The processing device according to claim 42, wherein said logic circuit is an arithmetic logic circuit capable of selectively executing a plurality of multi-bit operations.

44. (New) A processing device, comprising:

a reconfigurable circuit capable of arranging a circuit that can be divided into at least three divided circuits successively on a same region in an order of a first divided circuit, a second divided circuit, and a third divided circuit;

a memory portion storing an output of said reconfigurable circuit;

a state holding portion operating faster than said memory portion, and storing an output of said reconfigurable circuit; and

a switching portion selecting an output of said memory portion and an output of said state holding portion, and supplying the selected output to said reconfigurable circuit; wherein

said third divided circuit can be further divided into a fourth divided circuit and a fifth divided circuit, and allows arrangement successively on a same region in an order of said fourth divided circuit and said fifth divided circuit,

when said fourth divided circuit is arranged on said reconfigurable circuit, said switching portion supplies an output of said first and second divided circuits stored in said memory portion to said reconfigurable circuit, and

when said fifth divided circuit is arranged on said reconfigurable circuit, an output of said fourth divided circuit held in said state holding portion is supplied to said reconfigurable circuit.

45. (New) The processing apparatus according to claim 44, wherein

said reconfigurable circuit is configured as a combination circuit.

46. (New) The processing device according to claim 44, wherein

said reconfigurable circuit includes a plurality of logic circuits each capable of selectively executing a plurality of operation functions, and a connecting portion allowing setting of connection relation among the logic circuits.

47. (New) The processing device according to claim 46. wherein

said logic circuit is an arithmetic logic circuit capable of selectively executing a plurality of multi-bit operations.

48. (New) The processing device according t.o claim 44, wherein

said processing device is a digital demodulating device,

said first dividing circuit is a filter circuit processing an I signal,

said second divided circuit is a filter circuit processing a Q signal,

said third divided circuit is a demodulating circuit including a loop filter, a multiplier, and a positive/negative determining circuit.